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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/035,580
Filing Date: December 28, 2001
Appellant(s): STEELE, GUY L.

Guy L. Steele, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/07/2006 appealing from the Office action mailed 04/08/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The Appeal of In re Application of Guy Steele, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy Steele, Jr., U.S. Patent Application No. 10/035,595, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy Steele, Jr., U.S. Patent Application No. 10/035,584, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy Steele, Jr., U.S. Patent Application No. 10/035,587, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy Steele, Jr., U.S. Patent Application No. 10/035,647, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy Steele, Jr., U.S. Patent Application No. 10/035,579, in which an Appeal Brief was filed concurrently herewith.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

A substantially correct copy of appealed claims 1-40 appears on pages i-ix of the Appendix to the appellant's brief. The minor errors are as follows:

Re claims 6-7, 9, 11, 22, 24, 35, and 37, the status identifier for these claims should be "Previously Amended".

Re claims 1-5, 8, 10, 12-21, 23, 25-34, 36, and 38-40, the status identifier for these claims should be "Original".

(8) Evidence Relied Upon

5,995,991	Huang et al.	11-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (U.S. 5,995,991).

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (U.S. 5,995,991).

Re claim 1, Huang et al. disclose in Figures 1 and 4 a system (e.g. abstract and Figure 4) for providing a floating point product (e.g. col. 7 lines 65-66 and output of component 114 in Figure 4 as multiplication result), comprising: an analyzer circuit (e.g. components 24 and 26 in Figure 1 as detectors for detecting special operand(s) from input x and y operands; components 116-2 and 118-2 in Figure 4; and col. 7 lines 10-17; and col. 3 lines 10-15) configured to determine a first status of a first floating point operand

(e.g. output of 116-2) and a second status of a second floating point operand (e.g. output of 118-2) based upon data within the first floating point operand and data within the second floating point operand respectively, and a results circuit coupled (e.g. components 114, 150, and 122 in Figure 4) to the analyzer circuit (e.g. 116-2 and 118-2) and configured to assert a resulting floating point operand containing the product (e.g. col. 7 lines 65-66) of the first floating point operand and the second floating point operand and a resulting status embedded (e.g. output of 150) within the resulting floating point operand.

Re claim 2, Huang et al. further disclose in Figures 1 and 4 the analyzer circuit further comprises: a first operand buffer (e.g. 112) configured to store the first floating point operand, a second operand buffer (e.g. 112) configured to store the second floating point operand, a first operand analysis circuit (e.g. 116-2) coupled to the first operand buffer, the first operand analysis circuit configured to generate a first characteristic signal having information relating to the first status (e.g. table 1 in col. 6); and a second operand analysis circuit (e.g. 118-2) coupled to the second operand buffer, the second operand analysis circuit configured to generate a second characteristic signal having information relating to the second status (e.g. table 1 in col. 6).

Re claim 3, Huang et al. further disclose in Figures 1 and 4 the first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer (e.g. 116-2 and 118-2).

Re claim 4, Huang et al. further disclose in Figures 1 and 4 the memory storage external to the first operand buffer and the second operand buffer is a floating-point status register (e.g. 112 for storing the status information as example of output of 150).

Re claim 5, Huang et al. further disclose in Figures 1 and 4 the results circuit further comprises: a multiplier circuit (e.g. 114 and col. 7 lines 65-66) coupled to the analyzer circuit (e.g. 116-2 and 118-2), the multiplier circuit configured to produce the product of the first floating point operand and the second floating point operand (e.g. output of 114), a multiplier logic circuit (e.g. 150) coupled to the analyzer circuit and configured to produce the resulting status based upon the first status and the second status (e.g. 150), and a result assembler coupled to the multiplier circuit and the multiplier logic circuit, the result assembler configured to assed the resulting floating point operand and embed the resulting status within the resulting floating point operand (e.g. 112).

Re claim 6, Huang et al. further disclose in Figures 1 and 4 the multiplier logic circuit is organized according to the structure of a decision table (e.g. table 1 in col. 6).

Re claim 7, Huang et al. further disclose in Figures 1 and 4 product of the first floating point operand and the second floating point operand is identical in all cases to the product that would be produced if the two operands were swapped (e.g. inherently and col. 7 line 65 is vice versa of line 66).

Re claim 8, Huang et al. further disclose in Figures 1 and 4 the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, division by zero status, an infinity status, and an inexact status (e.g. col. 7 lines 20-22).

Re claim 9, Huang et al. further disclose in Figures 1 and 4 the overflow status represents one in a group of a plus overflow (+OV) status and a minus overflow (-OV) status (e.g. col. 1 lines 55-60 and col. 7 lines 20-23).

Re claim 10, Huang et al. further disclose in Figures 1 and 4 the overflow status is represented as a predetermined non-infinity numerical value (e.g. table 1 in col. 6).

Re claim 11, Huang et al. further disclose in Figures 1 and 4 the underflow status represents one in a group of a plus underflow (+UN) status and a minus underflow (-UN) status (e.g. col. 1 lines 55-60 and col. 7 lines 20-23).

Re claim 12, Huang et al. further disclose in Figures 1 and 4 the underflow status is represented as a predetermined non-zero numerical value (e.g. table 1 in col. 6).

Re claim 13, Huang et al. further disclose in Figures 1 and 4 the invalid status represents a not-a-number (NaN) status due to an invalid operation (e.g. col. 6 lines 39-43).

Re claim 14, Huang et al. further disclose in Figures 1 and 4 the infinity status represents one in a group of a positive infinity status and a negative infinity status (e.g. col. 9 lines 25-30).

Re claim 15, it is a method claim of claim 1. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 16, it is a method claim of claim 2. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 17, it is a method claim of claim 3. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 18, it is a method claim of claim 4. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 19, it is a method claim of claim 5. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 20, it is a method claim of claim 7. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 21, it is a method claim of claim 8. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 22, it is a method claim of claim 9. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 23, it is a method claim of claim 10. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 24, it is a method claim of claim 11. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 25, it is a method claim of claim 12. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 26, it is a method claim of claim 13. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 27, it is a method claim of claim 14. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 28, it is a computer-readable medium claim of claim 1. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 29, it is a computer-readable medium claim of claim 2. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 30, it is a computer-readable medium claim of claim 3. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 31, it is a computer-readable medium claim of claim 4. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 32, it is a computer-readable medium claim of claim 5. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 33, it is a computer-readable medium claim of claim 7. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 34, it is a computer-readable medium claim of claim 8. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 35, it is a computer-readable medium claim of claim 9. Thus, claim 35 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 36, it is a computer-readable medium claim of claim 10. Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 37, it is a computer-readable medium claim of claim 11. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 38, it is a computer-readable medium claim of claim 12. Thus, claim 38 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 39, it is a computer-readable medium claim of claim 13. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 40, it is a computer-readable medium claim of claim 14. Thus, claim 40 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

(10) Response to Argument

A. The rejection of claims 1-40 under 35 U.S.C 102(b) as being anticipated by Huang et al.

The applicant argues in pages 8-9 that the cited reference by Huang et al. fails to teach or suggest all the limitations "an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first operand and data within the second floating point operand respectively; and a result circuit coupled to the analyzer circuit and configured to ... a resulting status embedded within the resulting floating point operand" (emphasis added) because Huang's "tag value" (alleged status) is not "data within the first floating-point operand and data within the second floating point operand". In addition, the applicant repeated argues that the tag value stored in the 116-2 is clearly not a data within operand value.

The examiner respectfully submits that Figure 4 of the primary reference by Huang et al. clearly disclose all the limitations cited above wherein the analyzer circuit is the logic that determines the x_tag and y_tag as the first and second respectively status of the first and second respectively floating point operand wherein the examiner interprets the tag and the floating-point value of the cited reference by Huang et al. as the floating-point operand of the present invention. Thus, the associated tag is considered as part of

data within the floating-point operand wherein the floating-point operand composes of the associated tag and the floating-point value. This configuration can be clearly seen in the Figure 1 of the present invention. In Figure 1 of present invention, the first operand is composed of S, exponent, fraction (high part), and flags wherein conventionally IEEE labels the S, exponent, and fraction as floating-point value/operand. Therefore, the first operand 11A as seen in Figure 1 of present invention is the same as the X operand 116 in Figure 4 of cited reference by Huang et al. In addition, the register 112 in Figure is a memory for storing all the operands X and Y wherein each operand composed of an associated tag and a floating-point value.

The applicant further argues in page 10 first paragraph that the cited reference by Huang et al. fails to disclose "a resulting status embedded within the resulting floating point operand" as recited by claim 1 because the teaching results by Huang are stored and loaded separately into the tag value portion and the operand value portion such teachings by Huang et al. do not constitute a teaching or suggestion of "a resulting status embedded within the resulting floating point operand".

The examiner respectfully submits that the present claims do not clearly define or clarify how or where the resulting status is embedded within the resulting floating point operand. Based upon the Figure 4 and its corresponding specification portion of the instant applications, the claimed "embedded within" corresponds to appellant's diclosed attaching the resulting status to the resulting floating point value as clearly seen in Figure 1 of present invention. Given the case, Figure 4 of the cited reference by Huang clearly

and expressively discloses or teaches a resulting status (e.g. output of component 150 label as res_tag in Figure 4) embedded within (e.g. save, store, or attach along with result output of component 122 in Figure 4) the resulting floating point operand (e.g. output of component 122 as floating-point value in Figure 4).

(11) Related Proceeding(s) Appendix and Evidence Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Further, no evidence in addition to those already of record is identified in the Evidence Appendix.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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